WHAT IS CLAIMED IS:

1. An integrated circuit package comprising:

a silicon die having a first thickness;

a metallized polymer layer having a first side and a second side; and

a transition medium disposed between the silicon die and the first side of the metallized polymer layer wherein the transition medium has a second thickness, and the first thickness of the silicon die is less than the second thickness.

2. The integrated circuit package of claim 1 wherein the transition medium is nonconductive.

3. The integrated circuit package of claim 1 comprising a plastic encapsulant which encapsulates the silicon die and the transition medium, the plastic encapsulant having a coefficient of thermal expansion between approximately $7 \times 10^{-6}$/°C and $15 \times 10^{-6}$/°C.

4. The integrated circuit package of claim 1 wherein the transition medium comprises a mold compound material, a BT resin compound, a FR-4 compound, or a FR-5 resin compound.

5. The integrated circuit package of claim 1 wherein the transition medium has a coefficient of thermal expansion between approximately $7 \times 10^{-6}$/°C and $17 \times 10^{-6}$/°C.

6. The integrated circuit package of claim 1 wherein the presence of the transition medium reduces stress and fracture damage to the silicon die.

7. The integrated circuit package of claim 1 wherein a thickness of the metallized polymer layer and a thickness of the plastic encapsulant define a package thickness, wherein the silicon die is disposed near the middle of the package thickness.

8. The integrated circuit package of claim 7 wherein the package thickness is approximately 0.060 inches or less.

9. The integrated circuit package of claim 5 wherein the silicon die thickness is less than approximately 6 mils.

10. The integrated circuit package of claim 1 wherein the silicon die is coupled to the transition medium through an adhesive.

11. The integrated circuit package of claim 1 wherein a coefficient of thermal expansion for the adhesive is approximately 58 x $10^{-6}$/°C.

12. The integrated circuit package of claim 1 wherein the integrated circuit metallized polymer layer is a tape carrier having a dielectric layer and a conductive layer.

13. The integrated circuit package of claim 12 comprising solder balls mounted to the second side of the metallized polymer layer, the solder balls electrically contacting an etched circuit in a conductive layer of the tape carrier.

14. The integrated circuit package of claim 13 wherein the solder balls electrically connect the integrated circuit package to a printed circuit board.

15. The integrated circuit package of claim 14 wherein the solder balls are arranged in a grid fashion underneath the position for the silicon die.

16. The integrated circuit package of claim 1 wherein the cross sectional area of the silicon die is substantially less than or equal to the cross sectional area of the rigid transition medium.

17. The integrated circuit package of claim 1 wherein the cross sectional area of the silicon die is larger than the cross sectional area of the transition medium.

18. The integrated circuit package of claim 1 wherein the package is a BGA package.

19. The integrated circuit package of claim 1 wherein a volume of the silicon die is less than the volume of the rigid transition medium.

20. An integrated circuit package comprising:

a metallized polymer layer defining a first thickness;

a transition medium coupled to the metallized polymer layer;

a die coupled to the transition medium; and

a mold cap encapsulating the transition medium and the die, the mold cap defining a second thickness, wherein the first thickness and second thickness define a package thickness, wherein the die is disposed near the middle of the package thickness.

21. The integrated circuit package of claim 20 wherein the mold cap has a coefficient of thermal expansion similar to a coefficient of thermal expansion of the transition medium.

22. The integrated circuit package of claim 20 wherein the die is mounted to the transition medium with a layer of adhesive.

23. The integrated circuit package of claim 20 wherein the transition medium comprises a mold cap material, a second layer of adhesive, an elastomer, a BT resin compound, a FR-4 compound, or a FR-5 resin compound.

24. The integrated circuit package of claim 20 wherein the metallized polymer layer is a tape carrier.

25. An integrated circuit package comprising:

a tape carrier;

a first adhesive layer disposed on the tape carrier, the first adhesive layer having a coefficient of thermal expansion;

a transition medium having a first surface and a second surface, wherein the first surface of the transition medium engages the first adhesive layer, the transition medium having a coefficient of thermal expansion;

a second adhesive layer disposed on the second surface of the transition medium, the second layer of adhesive having a coefficient of thermal expansion; and

a die disposed on the second adhesive layer; and

a mold cap encapsulating the first adhesive layer, the transition medium, the second adhesive layer and the die, wherein the mold cap and tape carrier define a package thickness, wherein the transition medium and the mold cap have approximately the same coefficient of thermal expansion so as to reduce the thermal stress on the die during thermal cycling.

26. A method of packaging an integrated circuit comprising:

providing a silicon die adhered to a rigid transition medium;

applying a layer of adhesive to a tape carrier;

mounting the die and transition medium to the adhesive on the tape carrier; and

encapsulating the die and transition medium.

27. The method of claim 26 comprising electrically connecting the tape carrier to a printed circuit board with a solder ball.

28. The method of claim 26 wherein the providing step is carried out by cutting a semiconductor wafer adhered to a transition medium.

29. The method of claim 28 wherein the transition medium is approximately the same size and shape of the semiconductor wafer.

30. The method of claim 26 further comprising lapping the die to reduce the thickness of the die.

31. The method of claim 30 wherein the die is thinner than the transition medium.

32. A method of forming an integrated circuit package comprising:

providing a metallized polymer layer;

attaching a rigid transition medium layer to the metallized polymer layer using a first adhesive layer; and

coupling an integrated circuit die to the rigid transition medium using a second adhesive layer.

33. The method of claim 32 wherein attaching step is carried out with a material comprising mold compound, BT resin, FR-4 resin, or FR-5 resin.

34. The method of claim 32 wherein the attaching step is carried out with a rigid transition medium having a thickness between about 4 mils to about 8 mils.

35. A method of fabricating an integrated circuit comprising:

providing a semiconductor wafer;

attaching the semiconductor wafer to a transition medium using a first adhesive;

cutting a die from the semiconductor wafer, wherein the die is attached to a corresponding area of the transition medium; and

mounting the die and transition medium to a tape carrier.

36. The method of claim 35 wherein the cutting step is carried out by mechanical sawing, laser sawing, punching, or shearing.

37. The method of claim 35 comprising lapping the semiconductor wafer prior to the cutting step.

38. The method of claim 37 wherein the die thickness is reduced to less than approximately 6 mils.

39. The method of claim 35 wherein the attaching step is carried out with a transition medium having a coefficient of thermal expansion between about $7 \times 10^{-6}$/°C and $17 \times 10^{-6}$/°C.

40. The method of claim 35 wherein the attaching step is carried out with a rigid transition medium having a thickness between about 2 mils and 8 mils.

41. The method of claim 35 wherein the transition medium comprises a mold compound material, a BT resin compound, a FR-4 resin compound, or FR-5 resin compound.

42. The method of claim 35 wherein the thickness of the die, adhesive and transition medium is less than approximately 18 mils.

43. The method of claim 35 wherein a coefficient of thermal expansion for the adhesive is about $58 \times 10^{-6}$/°C.

44. A method of forming an integrated circuit package comprising:

providing a tape carrier;

providing a silicon die; and

reducing a thermal mismatch stress between the die and the integrated circuit package by disposing a rigid transition medium between the tape carrier and the silicon die.

45. A method of forming a package comprising:

placing a die on a pre-formed pedestal on a substrate; and

encapsulating the die and pedestal with a mold compound.

46. The method of claim 45 wherein the pre-formed pedestal comprises the same material as the mold compound.

47. The method of claim 45 wherein the placing step is performed without an adhesive.

48. The method of claim 45 wherein the pre-formed pedestal and the mold compound have a similar CTE.

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